(19) Europäisches Patentamt
European Patent Office
Office européen des brevets

(11) Publication number: 0 357 333 A2

(12) EUROPEAN PATENT APPLICATION

(21) Application number: 89308585.4

(22) Date of filing: 24.08.89

(51) Int. Cl.5: G 11 C 16/02
G 11 C 7/00

(30) Priority: 01.09.88 US 240830

(43) Date of publication of application:
07.03.90 Bulletin 90/10

(84) Designated Contracting States:
CH DE FR GB IT LI NL

(71) Applicant: ATMEL CORPORATION
2095 Ringwood Avenue
San Jose California 95131 (US)

(72) Inventor: Wu, Tsung-Ching
2458 Wooding Court San Jose
Santa Clara California 95128 (US)

Hu, James Cheng
12611 Wardell Court Saratoga
Santa Clara California 95070 (US)

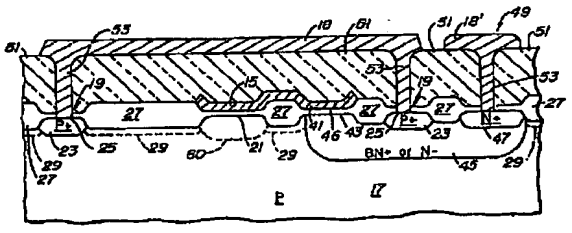
Huang, John Y.
44659 Park Meadow Drive Fremont
Alameda California 94539 (US)

(74) Representative: Purvis, William Michael Cameron et al
D. Young & Co. 10 Staple Inn
London WC1V 7RD (GB)

(54) Sealed charge storage structure.

(57) A memory cell in an EPROM device is totally sealed from ultraviolet light by a conductive cover (18) without openings therein for leads to the cell's drain, source and gate. Electrical communication with the source (18) is provided by direct contact with the conductive cover (18). Access to the drain and the floating gate (15) is provided by buried N+ implants (45), buried N+ layers or N-wells crossing underneath the sides of the cover (18). The memory cell has a single poly floating gate (15) rather than a stacked floating gate/control gate combination. The buried N+ implant or N-well (45) serves as the control gate and is capacitively coupled to the floating gate (15) via a thin oxide layer (43) in a coupling area (46).

FIG. 2.



EP 0 357 333 A2

Description

SEALED CHARGE STORAGE STRUCTURE

The invention relates to charge storage constructions, and in particular to nonvolatile, semiconductor memory devices employing floating gate memory cells.

In erasable programmable read-only memory (EPROM) devices, it is often desirable to have some memory cells completely sealed from ultraviolet light or other radiant energy so that these cells can store charge in their floating gates permanently. These cells are programmable read-only devices, i.e. non-erasable. This is usually accomplished with a layer of ultraviolet blocking material, such as metal, silicon or polysilicon, covering a memory cell to prevent the floating gate of the memory cell from being exposed to ultraviolet light. Like other memory cells on the EPROM device, the shielded memory cells are programmable by injecting charges into their floating gates. However, unlike the unshielded EPROM cells, the shielded memory cells should not be erasable when the device is flood exposed to ultraviolet light. The shielded memory cells operate, in effect, like a fusible PROM. Patent Specifications US-A-4,519,050 and US-A-4,530,074 to Folmsbee disclose EPROM devices having a radiative shield covering some memory cells, thereby inhibiting them from being erased and thereby enabling them to be permanently programmed. In an article entitled "An 80ns Address-Date Multiplex IMb CMOS EPROM", 1987 IEEE Int'l Solid State Circuits Conference, p. 70-71, M. Yoshida et al. describe, in Figure 5, an EPROM with a sub-surface contact to a cover material. However, the cover has an opening for emergence of a control gate.

In order to be useful, each memory cell in an EPROM, whether shielded or not, needs three connections, one each for source, drain and control gate, to the rest of the memory circuit. Otherwise, the cell would be inaccessible. For the shielded memory cells, these three connections typically require openings in the shield for the poly or other conductive leads, such as diffused or metal leads. Thus the shielded memory cells will have gaps or light paths where ultraviolet light may leak in and possibly cause accidental erasure of information stored as charges on the floating gates. Even where the openings through the shield are isolated from the cell area by a zig-zag shaped shield so as to provide a tortuous path for attenuating light, under flood exposure to ultraviolet light it is still possible that some shielded memory cells may be accidentally erased.

According to one aspect of the invention there is provided a semiconductor charge storage structure comprising,
a semiconductor substrate and a first electrode defined within the substrate,
an electrically floating second electrode disposed above the substrate in electron injection communication relation relative to the first electrode, whereby the second electrode stores accumulated electron charges,
radiation shielding cover means, disposed over and around the floating second electrode and contacting the substrate in a ring surrounding the floating second electrode on all sides, completely enclosing the second electrode from the substrate upwardly in all directions totally to seal the second electrode from radiation, and
conductive means defined within the substrate to contact both the first electrode and an electron charge source remote from the first electrode.

According to another aspect of the invention there is provided a sealed memory cell in a nonvolatile memory chip, the chip containing a plurality of memory cells formed in memory cell areas of the chip, at least one of the memory cells being sealed from exposure to radiant energy, the sealed memory cell comprising,
a chip substrate,
a source, a drain and a floating gate defined in a memory cell area of the chip substrate,
a radiant energy shielding cover in contact with the substrate in a ring completely enclosing the memory cell area, the memory cell area being totally sealed over and around all sides of the memory area from radiant energy by the cover, and
means defined within the chip substrate electrically to connect the source, the drain and the floating gate with corresponding connection terminals outside of the memory cell area, the floating gate being capacitively coupled to its corresponding connection terminal.

According to yet another aspect of the invention there is provided a sealed memory cell in an EPROM device, the EPROM device having a substrate with a plurality of floating gate memory cells formed in memory cell areas of the substrate, at least one of the memory cells being sealed from erasure by ultraviolet light, the sealed memory cell comprising,
spaced apart implants in a memory cell area of a substrate, the implants defining a source and a drain,
a thin gate oxide layer disposed over the substrate between the source and drain implants,
a polysilicon layer defining a floating gate, the polysilicon layer being disposed over the thin gate oxide layer and extending therefrom to a coupling area,
an ultraviolet-shielding electrically conductive cover disposed on top of the substrate with top and sides thereof respectively spaced over and around the source, the drain and the floating gate, the cover contacting the substrate in a ring completely surrounding the source, the drain and the floating gate whereby the memory cell is completely surrounded on top and sides by the cover,
electrically conductive channels defined in the substrate extending under the sides of the cover, a first of the channels extending from the drain implant in the memory cell area to a drain connection implant outside of the memory cell area, a second of the channels extending from the coupling area in the

memory cell area to a gate connection implant outside of the memory cell area, the coupling area having an oxide layer between the polysilicon layer and the second channel whereby the second channel is capacitively coupled to the floating gate, and

means for electrically connecting the source implant to the conductive cover, conductive lines of the EPROM device electrically communicating with the source, the drain and the gate via the respective conductive cover, drain connection implant and gate connection implant outside the memory cell area.

Such shielded memory cells in an EPROM device can be totally sealed from ultraviolet light, while still providing the necessary source, drain and gate connections to external circuitry.

Thus the memory cell is totally surrounded at the top and the sides by a conductive material cover, i.e. metal, silicon or polysilicon, and thus completely sealed from ultraviolet light, while access to the drain and the floating gate is provided by a conductive channel, such as an N+ diffusion or a buried N+ implant, in the substrate crossing underneath the cover. Access to the source is provided by direct contact with the conductive cover. Because of this undercross diffusion or implant there is no need for openings in the cover or shield to allow passage of conductive lines from the source, drain and gate terminals, since all terminals are effectively moved to outside the cover. The memory cell is completely sealed and no ultraviolet light can leak in to the floating gate.

An additional advantage of using a diffusion or implant to provide access to the floating gate, is that the memory cell does not require a double polysilicon stacking arrangement for the gate. Only a single polysilicon deposition is needed to form the memory cell. Essentially this arrangement includes a first electrode, such as a control gate, defined within the semiconductor substrate, and an electrically floating second electrode disposed above the substrate in electron injection communication with the first electrode, whereby the second electrode, such as the above-noted floating gate, stores accumulated charges. Means may be defined within the substrate to contact the first electrode with a terminal outside of a radiation shielding cover enclosing the floating second electrode or with the cover itself, so that the charge in the floating electrode may be sensed by external circuitry. Additional electrodes, such as a drain and source, may also be provided, or not, depending on the particular storage structure.

The invention is diagrammatically illustrated by way of example in the accompanying drawings, in which:-

Figure 1 is a top plan of a sealed memory cell according to the invention;

Figure 2 is a side section taken on line 2-2 in Figure 1, and illustrating an external gate connection for the memory cell;

Figure 3 is a side section taken on line 3-3 in Figure 1, and illustrating an external drain connection for the memory cell; and

Figure 4 is a top plan of an alternate floating gate configuration for use with a memory cell of the invention.

With reference to Figures 1 to 3, a sealed memory cell embodied in an EPROM device, comprises a source 11, a drain 13 and a floating gate 15 disposed on a semiconductor material substrate 17. The floating gate 15 is shielded from ultraviolet light and other radiant energy by a cover 18 completely surrounding and sealing in the memory cell at the top and the sides. The semiconductor material, typically silicon, of the substrate 17 blocks ultraviolet light and other radiant energy incident at the bottom of the EPROM device.

Typically, the substrate 17 is composed of a p-type (100)-oriented monocrystalline silicon material doped to a level sufficient to provide a resistivity in a range from 5 to 50 ohm-cm. The entire EPROM device, including the sealed memory cells, is made by a conventional CMOS N-well process with N-channel memory cells. The remainder of the EPROM device, including unsealed EPROM cells, N- and P-channel transistors and associated conductive circuitry, is not shown since it is completely conventional in both structure and fabrication.

The source 11 and the drain 13 areas typically comprise arsenic N+ diffusion implants. The arsenic implantation dose is about 4 -6 x $10^{15}/cm^2$. The floating gate 15 typically comprises a polysilicon layer with a thickness in a range of 2000 - 2600 Å and preferably less than 2400 Å thick. The floating gate polysilicon is formed over a gate oxide layer 21 about 300 - 350 Å thick and is doped with phosphorus to a concentration of about $10^{20} - 10^{21}/cm^3$ so as to reduce its sheet resistance to 15 - 40 ohm. As is conventional, a boron implant may be provided in the memory cell areas to adjust threshold.

The radiation shield or cover 18 is typically composed of a conductive material such as aluminium or another metal. Alternatively, silicon substrate material polysilicon which has been p-type doped, such as with boron, may be used. The conductive cover 18 contacts a P+ diffusion ring 23 and the source 11 by contact regions 19 and 31. The contact region 19 is a ring shaped contact to the P^+ diffusion ring 23 only. The radiation cover 18 is oversize relative to the outer perimeter of the contact region 19. The ring 23 completely surrounds the memory cell. The ring 23 can also be an N+ ring except in areas discussed below where there is a buried N+ or N-well crossing. Those cross areas of the ring 23 must be p-type. A 0.8 - 1.2 micron thick field oxide layer 27 with field boron implant channel stops 29 is provided around memory cell elements wherever electrical isolation is needed.

In order to provide electrical access to the source 11, the drain 13 and the floating gate 15 without providing openings in the cover 18, electrically conductive channels are provided which cross under the P+ ring 23. Access to the source 11 may be achieved via the direct contact region 31 with the cover 18. It may also be achieved with an N-well, buried N+ implant or buried N+ layer, similar to a layer 35 in the drain connection, described below.

Access to the drain 13 is provided by an N-well, buried N+ implant or the buried N+ layer 35 extending from the N+ drain implant 13 underneath

the P+ ring 23 and the cover 18 to an N+ drain connection diffusion implant 37 on the outside of the memory cell, i.e. outside the P+ ring 23. A metal terminal 18 fills up a contact hole 39 and makes contact with the drain connection implant 37.

Access to the floating gate 15 is also provided by means of a conductive channel extending under the P+ ring 23 and the cover 18. The floating gate 15 is a piece of polysilicon with an elongate portion extending over the gate oxide layer 21 above the gap or channel between the source 11 and the drain 13 and a larger coupling portion 41 lying over a surface coupling area 46 of the buried N+ layer, buried N+ implant or N-well 45. A channel implant 60 under the gate oxide layer 21 is used to adjust the threshold voltage of the memory cell. The thick field oxide layer 27 with the channel stop implant 29 separates the actual gate area between the source 11 and the drain 13 and the coupling area 46. The coupling portion 41 of the floating gate polysilicon may be a square or rectangular piece as shown in Figure 1 or may be a fork-like coupling portion 141, as in Figure 4, with several finger projections 143. The shape of the coupling portion 41 or 141 may be varied so as to vary the capacitance of the coupling. A thin oxide layer 43, typically 300 - 350 Å thick is disposed between the coupling portion 41 or 141 of the floating gate 15 and the surface area 46 of the buried N+ layer, the buried N+ implant or the N-well 45, which in turn extends under the P+ ring 23 and the cover 18 to an N+ control gate connection diffusion implant 47 outside of the memory cell of the P+ ring 23. A metal terminal 18' fills up a contact opening 49 and makes contact with the control gate connection implant 47.

The EPROM device structures, such as the source 11, the drain 13, the drain connection 37, the floating gate 15 and the control gate connection implant 47 of the sealed memory cells, are covered with boron/phosphorus-doped silicon glass (BPSG) 51 and contact holes 53 are opened in the glass for the necessary conductive connections, such as the sides of the cover 19 and the metal drain and gate connections 39 and 49. Phosphorus-doped silica glass (PSG) may also be used. The top of the cover 18 is deposited on top of the BPSG 51. Prior to this deposition, the EPROM device may be exposed to ultraviolet light to remove any residual charges stored in the floating gate 15 during fabrication. Other conductive lines, not shown, connect to the source, and the drain and gate connections 18, 39 and 49, and form part of the overall EPROM circuit. More than one layer of conductive lines separated by an intermetal insulative layer may be necessary.

The sealed memory cell is programmed by injecting charges into the floating gate 15 by way of electron injection across the thin oxide layer 21 or by hot electron injection through the oxide layer 21. Typically, the source 11 is placed at ground potential via the cover 18, the drain 13 is placed at 12 volts potential or higher via the drain connection 39, and the control gate, represented by the control gate connection 47, the buried N+ implant 45 and the surface area 46, is placed at 12 volts potential or higher via the gate connection 49. The control gate capacitively couples to the floating gate 15 via the surface area 46, the thin oxide layer 43 and the coupling area 41 or 141. Though in structure it is quite different, in normal operation the memory cell described is equivalent to the regular EPROM cell with stacked gates, and is read in the same manner. The only operational difference is that the sealed memory cell cannot be erased. The buried channels enable electrical communication with the drain, the source and the gate elements of the memory cell without the previously necessary openings in the cover 18. Thus, ultraviolet light cannot leak into the memory cell and cause accidental erasure.

While the invention has been described with respect to memory cells, other charge storage structures might need to be shielded from light or other radiation. In such a situation, the electrode contact construction of the invention may be employed. The shield material would be appropriate for blocking the undesired radiation.

Claims

1. A semiconductor charge storage structure comprising, a semiconductor substrate (17) and a first electrode (46) defined within the substrate,
an electrically floating second electrode (15) disposed above the substrate (17) in electron injection communication relation relative to the first electrode (46), whereby the second electrode (15) stores accumulated electron charges,
radiation shielding cover means (18), disposed over and around the floating second electrode (15) and contacting the substrate (19) in a ring surrounding the floating second electrode on all sides, completely enclosing the second electrode from the substrate upwardly in all directions totally to seal the second electrode from radiation, and
conductive means defined within the substrate (17) to contact both the first electrode (46) and an electron charge source remote from the first electrode (46).

2. A sealed memory cell in a nonvolatile memory chip, the chip containing a plurality of memory cells formed in memory cell areas of the chip, at least one of the memory cells being sealed from exposure to radiant energy, the sealed memory cell comprising,
a chip substrate (17),
a source (11), a drain (13) and a floating gate (15) defined in a memory cell area of the chip substrate (17),
a radiant energy shielding cover (18) in contact with the substrate (17) in a ring (19) completely enclosing the memory cell area, the memory cell area being totally sealed over and around all sides of the memory area from radiant energy by the cover (18), and
means (31, 35, 45) defined within the chip substrate electrically to connect the source (11), the drain (13) and the floating gate (15)

with corresponding connection terminals (39, 49) outside of the memory cell area, the floating gate (15) being capacitively coupled to its corresponding connection terminal (49).

3. A sealed memory cell according to claim 2, wherein the connecting means comprises,
a first electrically conductive channel (35) within the substrate extending from the drain (13) in the memory cell area, under the shielding cover (18), to a corresponding drain connection terminal (39),
a second electrically conductive channel (45) within the substrate extending from a capacitive coupling area (46) located beneath an extension (41, 141) of the floating gate (15), under the shield cover (18), to a corresponding gate connection terminal (49), and
a conductive line (31) electrically contacting the source (11) and the cover (18), the cover (18) being electrically conductive.

4. A sealed memory cell according to claim 3 wherein the first (35) and second (45) conductive channels comprise N-wells, buried N+ implant or buried N+ layers.

5. A sealed memory cell according to claim 3, wherein the floating gate extension (41) above the capacitive coupling area (46) has a polygonal shaped.

6. A sealed memory cell according to claim 3, wherein the floating gate extension (141) above the capacitive coupling area (46) has a forked shaped with a plurality of fingers.

7. A sealed memory cell according to claim 2, wherein the cover (18) is composed of metal, polysilicon or monocrystalline silicon.

8. A sealed memory cell in an EPROM device, the EPROM device having a substrate with a plurality of floating gate memory cells formed in memory cell areas of the substrate, at least one of the memory cells being sealed from erasure by ultraviolet light, the sealed memory cell comprising,
spaced apart implants in a memory cell area of a substrate, the implants defining a source (11) and a drain (13),
a thin gate oxide layer (21) disposed over the substrate between the source and drain implants,
a polysilicon layer defining a floating gate (15), the polysilicon layer being disposed over the thin gate oxide layer (21) and extending therefrom to a coupling area (46),
an ultraviolet-shielding electrically conductive cover (18) disposed on top of the substrate with top and sides thereof respectively spaced over and around the source (11), the drain (13) and the floating gate (15), the cover (18) contacting the substrate in a ring (23) completely surrounding the source (11), the drain (13) and the floating gate (15) whereby the memory cell is completely surrounded on top and sides by the cover (18),
electrically conductive channels (35, 45) defined in the substrate extending under the sides of the cover (18), a first (35) of the channels extending from the drain implant (11) in the memory cell area to a drain connection implant (37) outside of the memory cell area, a second (45) of the channels extending from the coupling area (46) in the memory cell area to a gate connection implant (47) outside of the memory cell area, the coupling area (46) having an oxide layer (43) between the polysilicon layer and the second channel (45) whereby the second channel (45) is capacitively coupled to the floating gate (15), and
means for electrically connecting the source implant to the conductive cover (18), conductive lines of the EPROM device electrically communicating with the source (11), the drain (13) and the gate (15) via the respective conductive cover, drain connection implant (37) and gate connection implant (47) outside the memory cell area.

9. A sealed memory cell according to claim 8, wherein the electrically conductive channels (35, 45) are N-wells, buried N+ implants or buried N+ layers.

10. A sealed memory cell according to claim 8, wherein the polysilicon layer (41) over the coupling area has a polygonal shape.

11. A sealed memory cell according to claim 8, wherein the polysilicon layer (141) over the coupling area has a forked shape with a plurality of fingers (143) disposed over the second channel (45).

12. A sealed memory cell according to claim 8, wherein the cover (18) is composed of metal, polysilicon or monocrystalline silicon.

13. A sealed memory cell according to claim 8, wherein the connecting means comprises a conductive layer (31) disposed over and contacting the source implant (11), the conductive layer (31) also contacting a side of the conductive cover (18).

14. A sealed memory cell according to claim 8, wherein the source (11) and drain (13) are defined by arsenic N+ implants.

15. A sealed memory cell according to claim 8, wherein a ring implant (23) is disposed in the substrate beneath the sides of the cover (18), the channels (35, 45) crossing under the ring implant (23) in crossing regions, the ring implant (23) being a P+ implant at least in the crossing regions.

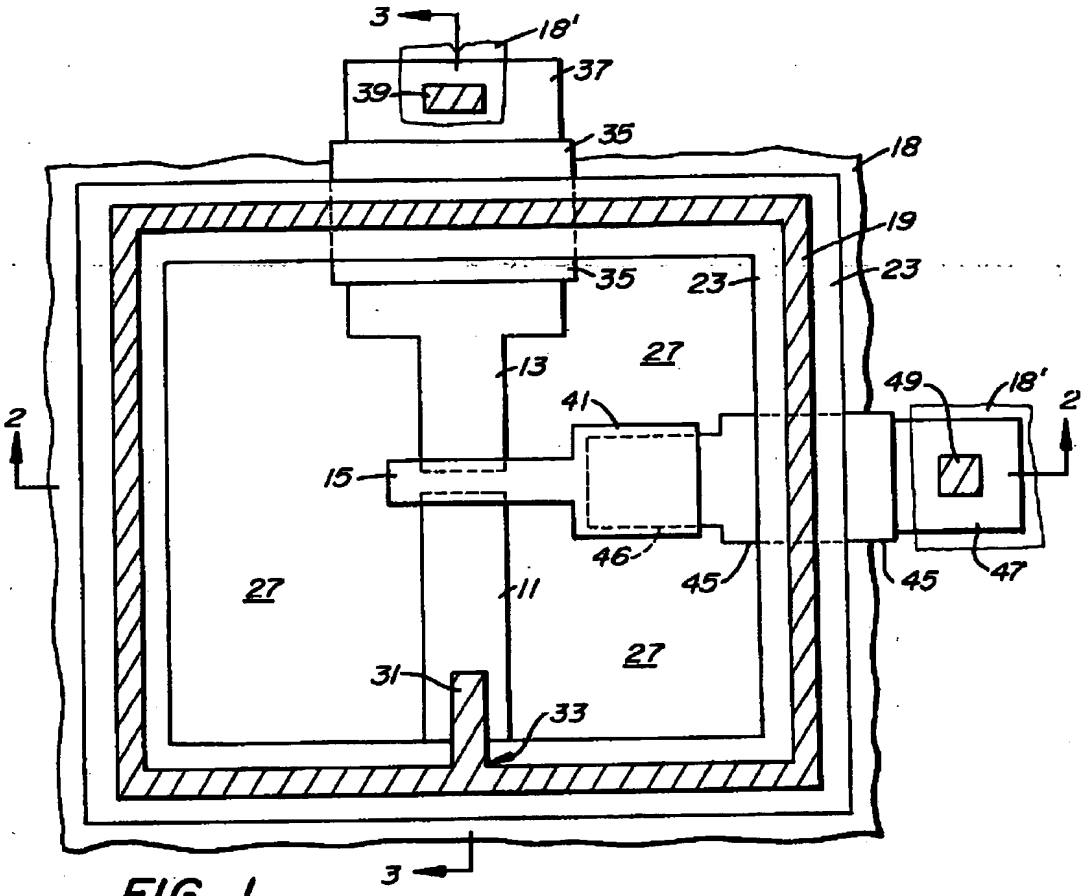

3
18'
37
39
35
18
19
23
35
23
27
13
41
49
18'
2
2
15
46
45
45
47
27
11
27
31
33
3

FIG._1.

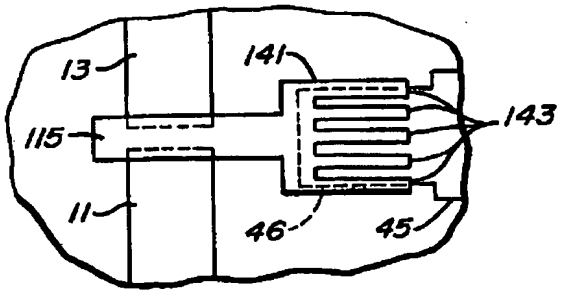

13
141
143
115
11
46
45

FIG._4.

FIG._2.

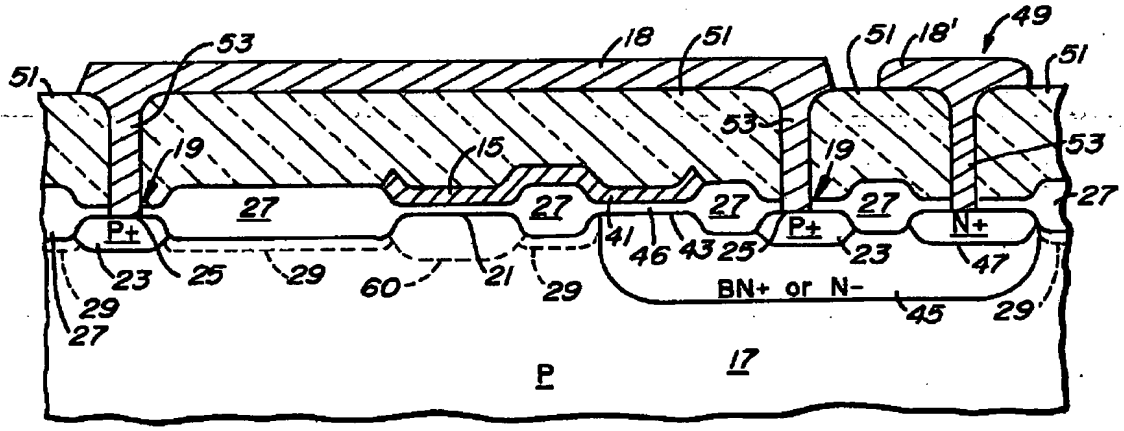
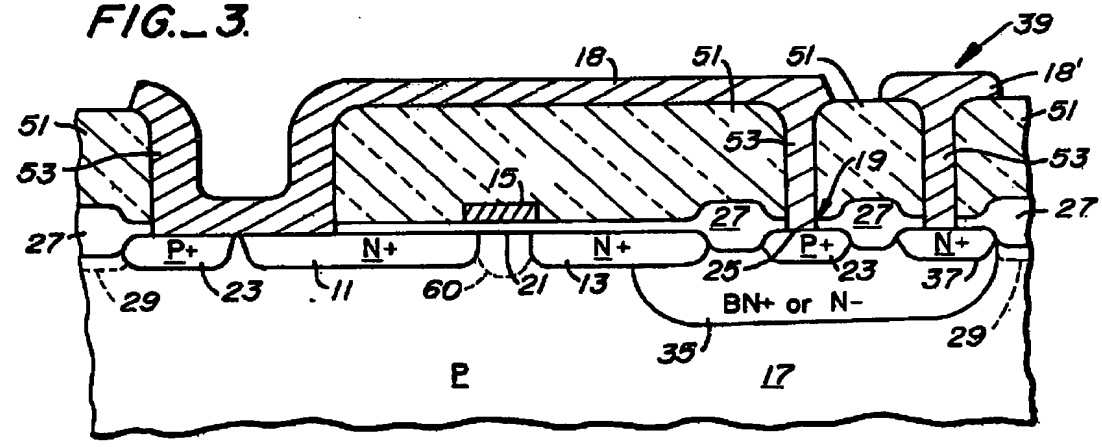

53
18
51
51
18'
49
51
51
19
15
53
19
53
27
27
27
27
27
P+
P+
N+
41
46
43
25
23
47
23
25
29
60
21
29
BN+ or N-
45
29
29
27
P
17

FIG._3.


39
18
51
51
18'
51
51
53
53
19
15
53
27
27
27
27
P+
N+
N+
P+
N+
25
23
37
29
23
11
60
21
13
BN+ or N-
29
35
P
17